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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VIDWAN, JASJIT S	

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,419	GEHMAN ET AL.	
	Examiner	Art Unit	
	JASJIT S. VIDWAN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Remarks, filed 12/22/08, with respect to the rejection(s) of claim(s) 1 & 16 under Paul & Dickie have been fully considered and are persuasive. Applicant in the request had argued two points (1) the art rejection for claim 1 by Paul and Dickie, particularly the limitations of (a) the software layer adapted to configured multiple instantiations of a peripheral device within an integrated circuit by Paul and (b) the software layer defining offset values for registers of the peripheral device and defining a data structure for the peripheral device by Dickie; and (2) improper obviousness for combining the references. The Pre-Appeal conference agreed that the Examiner has made reasonable rejection for points 1a and 2 as raised by the Applicant. However, it was unclear how the secondary reference by Dickie would meet/anticipated the missing limitations from the primary reference by Paul; specifically the software layer defining offset values for registers of the peripheral device and defining a data structure for the peripheral device as argued by the application. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Paul in view of xxxx.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 & 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul et al, U.S. Patent No: 6,466,972 **[herein after Paul]** and further in view of Wisor et al, U.S. Patent No: 6,021,498 **[hereinafter Wisor]**.

4. **As per Claims 1 & 16**, Paul teaches a reusable software block **[see Abstract, "…templates called machine classes, which can be used to manage a set of similar machines."]** stored in a

computer-readable memory **[see Abstract, "…stored permanently in a database"]**, the reusable software block comprising:

i. Device hardware abstraction software layer adapted to configure multiple instantiations of a peripheral device within an integrated circuit **[see Col. 2, Lines 48-63]**,

ii. Platform hardware abstraction software layer defining an address map of the system **[see Col. 9, Lines 16-28]**, the platform hardware abstraction software layer adapted to configure each instantiation of the peripheral device via calls to the device hardware abstraction software layer **[see Col. 10, Lines 19-26 – also see Col. 10, Lines 56 - Col. 11, Line 14].**

5. Paul teaches above limitations; however fails to explicitly disclose the process of configuring multiple instances of peripheral device to include defining offset values for registers of the peripheral device and defining a data structure for the peripheral device. Wisor teaches a well known method of defining offset values for registers of the peripheral device and defining a data structure for the peripheral device **[see Wisor, Col. 1, 26-38]**.

6. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above teachings in order to take advantage of effectively communicating with peripheral devices connected to the said system by designating the configuration registers of each instantiation of a peripheral. It if for this reason that one of ordinary skill in the art would have been motivated to combine the two teachings.

7. Claims 2-7 & 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul et al, U.S. Patent No: 6,466,972 **[herein after Paul]** and Wisor et al, U.S. Patent No: 6,021,498 **[hereinafter Wisor]** and further in view of Spencer et al U.S. Patent No: 6,044,225 **[hereinafter Spencer]**.

8. **As per Claim 2 & 17**, Paul as modified by Wisor teaches a reusable software block wherein the device hardware abstraction layer comprises Memory registers location adapted to the configurable during initialization of the system **[see Wisor, Col. 1, Lines 33-38]**

9. Paul and Wisor fail to teach said reusable software block having an abstraction later further comprising an interrupt configuration. Although it is obvious to one of ordinary skill in the art for peripheral devices to include configurable registers and interrupt configurations therein, Spencer teaches the said limitation of peripheral device having both including interrupt configuration which is configured for the peripheral device during the initialization of the system **[see Spencer, Col. 22, Lines 28-38]**.

10. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the two teachings in order to not only have a more efficient but also a device specific customizable peripheral communicating with the host system. It is for this reason that one of ordinary skill in the art would have been motivated to combine the two teachings.

11. **As per Claim 3 & 18**, Paul & Wisor as modified by Spencer above teaches a system wherein the memory register locations and the interrupt configurations define the structure of the peripheral device using variables **[See Spencer, Col. 22, Lines 38-46]**

12. **As per Claim 4, 5 & 19**, Paul & Wisor as modified by Spencer teaches a system wherein the platform hardware abstraction layer comprises a memory map of memory locations of the peripheral device corresponding to a particular implementation of the peripheral device, the memory map adapted to replace the variables with unique memory locations for each instantiation **[see Wisor, Fig. 1, element 120]**.

13. **As per Claim 6, 7 & 20**, Paul teaches a system wherein the configurable structure of the peripheral device is defined in the device hardware abstraction layer using variables, the platform hardware abstraction layer comprising an interrupt configuration corresponding to interrupt connections for a particular implementation of the peripheral device, the interrupt configuration adapted to replace the variables with unique interrupt connections for each instantiation **[see Spencer , Col. 22, Lines 28-46]]**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASJIT S. VIDWAN whose telephone number is (571)272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on 571.272.6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. S. V./
Examiner, Art Unit 2182

/Ilwoo Park/
Primary Examiner, Art Unit 2182
March 1, 2009